ANSYS

Minimize EMI by using an EMI aware design process

EMI is generally determined at the or close to the end of the design phase of a product. In order to minimize EMI this presentation proposes that EMI awareness is obtained during the design process, well before a design is fully finished. At the same time as designs are checked for Signal Integrity and Power Integrity, EMI insight and levels can also be determined for sections of a PCB or a design. Using ANSYS tools, EMI can be determined and reduced by properly addressing design issues that are actually part of SI or PI design concerns. This presentation will clearly show several EMI issues and how EMI can be minimized early in the design cycle by following good SI and PI guidelines.

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CPD Hour is available. Bring flyer for credit

September 18, 2014
5:30 – 7:30
(food and drink provided)
RSVP Early – Space is Limited

The Oak Barrel Brasserie and Taphouse
5975 Canal Rd.
Valley View, OH 44125
216.520.3640

IEEE Cleveland Section

RSVP to: http://www.clevelandieee.org/ansys-rsvp-sept2014

About the Presenter

Markus Kopp is a Lead Application Specialist for the ANSYS Electronics high frequency products, which includes tools such as HFSS, SIwave, and Designer. During the past 13 years, while working at ANSYS he has progressively held the roles of Application Engineer, Country Manager and Senior Application Specialist, focusing on the high-frequency simulation tools and markets.

This is to certify that _____ attended this seminar. Certified by _____. Certificate of attendance and other evidence of CPD activity should be retained by the attendee for auditing purposes.